CLAIMS

1. A device comprising:

an overflow generator to generate a plurality of overflow signals having a plurality of periods;

a plurality of control registers storing a plurality of selection values; and

a first trigger generator comprising first trigger generation means for generating a first timeout event trigger signal based on the plurality of overflow signals and a first one of the plurality of selection values.

2. The device of claim 1, wherein the plurality of control registers further stores a plurality of control values, and wherein the first trigger generation means comprises means for generating the first timeout event trigger signal based on the plurality of overflow signals, the first one of the plurality of selection values, and a first one of the plurality of control values.

3. The device of claim 1, further comprising:

a second trigger generator comprising second trigger generation means for generating a second timeout event trigger signal based on the plurality of overflow signals and a second one of the plurality of selection values.

4. The device of claim 3, wherein the plurality of control registers further stores a plurality of control values, and wherein the second trigger generation means comprises means for generating the second timeout event trigger signal based on the plurality of overflow signals, the second one of the plurality of selection values, and a second one of the plurality of control values.

5. The device of claim 1, wherein the first trigger generation means comprises:

means for identifying a first one of the plurality of overflow signals based on the first one of the plurality of selection signals;

means for identifying a period of the first one of the plurality of overflow signals; and

means for generating the first timeout event trigger signal based on the period of the first one of the plurality of overflow signals.

6. The device of claim 1, wherein the means for generating the first timeout event trigger signal based on the period of the first one of the plurality of overflow signals comprises means for asserting the first timeout event trigger signal if the period of the first one of the plurality of overflow signals has elapsed since the first trigger generator was last reset.

7. The device of claim 1, wherein the plurality of control registers further stores a plurality of control values, and wherein the first trigger generation means comprises:

means for identifying a first one of the plurality of overflow signals based on the first one of the plurality of selection signals; and

means for generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals.

8. The device of claim 7, wherein *C* is the first one of the plurality of control values, and wherein the means for generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals comprises:

means for asserting the first timeout event trigger signal if the first one of the plurality of overflow signals has been asserted at least *C*+1 times since a first predetermined reset event; and

means for deasserting the first timeout event trigger signal otherwise.

9. The device of claim 7, wherein *C* is the first one of the plurality of control values, wherein *P* is the period of the first one of the plurality of overflow signals, and wherein the means for generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals comprises:

means for asserting the first timeout event trigger signal if an amount of time at least equal to *PC* has elapsed since a predetermined reset event; and

means for deasserting the first timeout event trigger signal otherwise.

10. A device comprising:

an overflow generator to generate a plurality of overflow signals having a plurality of periods;

a plurality of control registers storing a plurality of selection values and a plurality of control values;

a first trigger generator comprising first trigger generation means for generating a first timeout event trigger signal based on the plurality of overflow signals, a first one of the plurality of selection values, and a first one of the plurality of control values; and

a second trigger generator comprising second trigger generation means for generating a second timeout event trigger signal based on the plurality of overflow signals, a second one of the plurality of selection values, and a second one of the plurality of control values.

11. A method comprising steps of:

(A) generating a plurality of overflow signals having a plurality of periods;

(B) generating plurality of selection values; and

(C) generating a first timeout event trigger signal based on the plurality of overflow signals and a first one of the plurality of selection values.

12. The method of claim 11, further comprising a step of:

(D) generating a plurality of control values; and

wherein the step (C) comprises a step of generating the first timeout event trigger signal based on the plurality of overflow signals, the first one of the plurality of selection values, and a first one of the plurality of control values.

13. The method of claim 11, further comprising a step of:

(D) generating a second timeout event trigger signal based on the plurality of overflow signals and a second one of the plurality of selection values.

14. The method of claim 13, further comprising a step of:

(E) generating a plurality of control values; and

wherein the step (D) comprises a step of generating the second timeout event trigger signal based on the plurality of overflow signals, the second one of the plurality of selection values, and a second one of the plurality of control values.

15. The method of claim 11, wherein the step (C) comprises steps of:

(C)(1) identifying a first one of the plurality of overflow signals based on the first one of the plurality of selection signals;

(C)(2) identifying a period of the first one of the plurality of overflow signals; and

(C)(3) generating the first timeout event trigger signal based on the period of the first one of the plurality of overflow signals.

16. The method of claim 15, wherein the step (C)(3) comprises a step of asserting the first timeout event trigger signal if the period of the first one of the plurality of overflow signals has elapsed since a first predetermined reset event.

17. The method of claim 11, further comprising a step of:

(D) generating a plurality of control values; and

wherein the step (C) comprises steps of:

(C)(1) identifying a first one of the plurality of overflow signals based on the first one of the plurality of selection signals; and

(C)(2) generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals.

18. The method of claim 17, wherein the first one of the plurality of control signals represents a value *C*, and wherein the step (C)(2) comprises steps of:

(C)(2)(1) asserting the first timeout event trigger signal if the first one of the plurality of overflow signals has been asserted at least (*C*+1) times since a first predetermined reset event; and

(C)(2)(2) deasserting the first timeout event trigger signal otherwise.

19. The method of claim 17, wherein the first one of the plurality of control signals represents a value *C*, wherein *P* is the period of the first one of the plurality of overflow signals, and wherein the step (C)(2) comprises steps of:

(C)(2)(1) asserting the first timeout event trigger signal if an amount of time at least equal to *PC* has elapsed since a predetermined reset event; and

(C)(2)(2) deasserting the first timeout event trigger signal otherwise.

20. A method comprising steps of:

(A) generating a plurality of overflow signals having a plurality of periods;

(B) generating plurality of selection values;

(C) generating a plurality of control values;

(D) generating a first timeout event trigger signal based on the plurality of overflow signals, a first one of the plurality of selection values, and a first one of the plurality of control values; and

(E) generating a second timeout event trigger signal based on the plurality of overflow signals, a second one of the plurality of selection values, and a second one of the plurality of control values.

21. A device comprising:

a multiplexer comprising a plurality of data inputs to receive a plurality of overflow signals, a selection input to receive a selection signal, and an output to provide one of the plurality of overflow signals selected by the selection signal;

a one-bit counter comprising a data input coupled to the output of the multiplexer, a reset input, and a data output to provide a one-bit count signal; and

an AND gate having a first input coupled to the data output of the one-bit counter, a second input coupled to the output of the multiplexer, and an output to provide a first timeout event trigger signal.

22. The device of claim 21, further comprising:

a latch comprising a data input coupled to the output of the AND gate, and an output to provide a second timeout event trigger signal.

23. A device comprising:

selection means comprising means for receiving a plurality of overflow signals, means for receiving a selection signal, means for selecting one of the plurality of overflow signals based on the selection signal, and means for providing as output the selected one of the plurality of overflow signals;

counting means for counting the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event; and

timeout event trigger signal generation means for asserting a timeout event trigger signal when the selected one of the plurality of overflow signals has been asserted twice since the predetermined reset event.

24. The device of claim 21, further comprising:

a latch comprising means for receiving a clock signal, means for receiving the first timeout event trigger signal, and means for providing the timeout event trigger signal as output in response to a transition in the clock signal.

25. A device comprising:

a multiplexer comprising a plurality of data inputs to receive a plurality of overflow signals, a selection input to receive a selection signal, and an output to provide one of the plurality of overflow signals selected by the selection signal;

a multi-bit counter comprising a data input coupled to the output of the multiplexer, a reset input, and a plurality of data outputs to provide a multi-bit count signal;

a multi-bit comparator having a first plurality of inputs coupled to the plurality of data outputs of the multi-bit counter, a second plurality of inputs to receive a multi-bit control signal, and a data output to provide a comparison signal indicating whether the multi-bit count signal is equal to the multi-bit control signal; and

an AND gate having a first input coupled to the data output of the multi-bit comparator, a second input coupled to the output of the multiplexer, and an output to provide a first timeout event trigger signal.

26. The device of claim 25, further comprising:

a latch comprising a data input coupled to the output of the AND gate, and an output to provide a second timeout event trigger signal.

27. A device comprising:

selection means comprising means for receiving a plurality of overflow signals, means for receiving a selection signal, means for selecting one of the plurality of overflow signals based on the selection signal, and means for providing as output the selected one of the plurality of overflow signals;

counting means for counting the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event;

comparison means for generating a comparison signal indicating whether a predetermined control value is at least equal to the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event; and

timeout event trigger signal generation means for asserting a timeout event trigger signal when the predetermined control value is at least equal to the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event.

28. The device of claim 27, further comprising:

a latch comprising means for receiving a clock signal, means for receiving the first timeout event trigger signal, and means for providing the timeout event trigger signal as output in response to a transition in the clock signal.

29. A method comprising steps of:

(A) receiving a plurality of overflow signals having a plurality of periods;

(B) receiving a first selection signal;

(C) identifying a first one of the plurality of overflow signals based on the first selection signal; and

(D) generating a first trigger signal based on the identified one of the plurality of overflow signals.

30. The method of claim 29, wherein the step (D) comprises a step of asserting the first timeout event trigger signal if an amount of time at least equal to the period of the first one of the plurality of overflow signals has elapsed since a first predetermined reset event.

31. The method of claim 29, further comprising a step of:

(E) receiving a first control signal; and

wherein the step (D) comprises a step of generating the first trigger signal based on the first control signal and the identified one of the plurality of overflow signals.

32. The method of claim 31, wherein the first one of the plurality of control signals represents a value *C*, and wherein the step (D) comprises steps of:

(D)(1) asserting the first timeout event trigger signal if the first one of the plurality of overflow signals has been asserted at least *C*+1 times since a first predetermined reset event; and

(D)(2) deasserting the first timeout event trigger signal otherwise.

33. The method of claim 31, wherein the first one of the plurality of control signals represents a value *C*, wherein *P* is the period of the first one of the plurality of overflow signals, and wherein the step (D) comprises steps of:

(D)(1) asserting the first timeout event trigger signal if an amount of time at least equal to *PC* has elapsed since a predetermined reset event; and

(D)(2) deasserting the first timeout event trigger signal otherwise.